REMARKS

Claims 6, 7, 13 and 14 were objected to. In response, claims 1 and 13 have been re-written in independent form. Claims 6, 7, 13 and 14 should each be allowable.

Claims 15-18 were rejected under 35 U.S.C. 103(a) as being anticipated by AAPA in view of Moshier (US 4,228,498), along with claims 1-5 and 8-12.

Claim 15 has been re-written to include subject matter similar to that found in allowed claim 6. Claims 15-18 should now also be in condition for allowance.

It is first noted that the instant specification does not specifically characterize any work done by another as "prior art", and thus for at least this reason is not seen to fall within MPEP section 2129, sub-sections I or II. As such, it is not admitted that the Examiner's rejection based in part on Applicant's Admitted Prior Art (AAPA) is warranted.

Moshier teaches a multibus processor that appears to function as a slave processor 12 for a host computer 28 (a PDP-11), and appears to be interfaced thereto via external control registers 26 (see Fig. 1) and, in Fig. 4, the instruction memory 68. Thus, while the terms "multibus" and "core" (col. 6, lines 26 and 27) appear in Moshier, any resemblance to the claimed invention is at most superficial.

Further, it is not understood where there would be a suggestion to employ the teachings of Moshier as it pertains to a multibus processor that operates under control of a host computer, such as a PDP-11 computer, in a system on a chip (Soc) architecture of a type generally discussed in the background of the instant specification.

In any event, claim 1 has been amended to recite:

> "A data processor comprising at least two processor cores, each said processor core having a first interface supporting a first bus coupled to an associated one of at least two program memories, a second interface supporting a second bus coupled to a common data memory accessible by each of said at least two processor cores, and a third interface supporting a third bus coupled to at least one input/output device accessible by each of said at least two processor cores, each of said first, second and third buses comprise an address bus that is sourced from one of said processor cores and a data bus."

There is clearly no disclosure of this type of architecture in the Moshier patent, and thus even if one was presented with a SoC architecture of a type generally described in the background of the instant patent application, there would be no guidance or suggestion or motivation to make the proposed combination. Further, even if the proposed combination were made as stated by the Examiner, which is not admitted is suggested, the resulting combination would clearly not suggest the subject matter found in claim 1, e.g., "at least two processor cores" each having a first interface "supporting a first bus coupled to an associated one of at least two program memories", a second interface "supporting a second bus coupled to a common data memory" and a third interface supporting "a third bus coupled to at least one input/output device accessible by each of said at least two processor cores", where each of the first, second and third buses "comprise an address bus that is sourced from one of said processor cores and a data bus". In that claim 1 is clearly patentable, then claims 2-5 and 8 are also patentable.

Claim 9 as filed includes recitations that are similar in some respects to those now found in claim 1, and should also be found to be patentable for at least this reason alone. In that claim 9 is clearly patentable, then claims 10-12 are also patentable.

The Examiner is respectfully requested to reconsider and remove the rejections of the claims, and to allow all of the pending claims as now presented for examination. An early notification of the allowability of claims 1-18 is earnestly solicited.